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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,274	06/19/2001	Toshifumi Oida	36856.517	1664

7590 12/16/2004

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EXAMINER	
KNOWLIN, THJUAN P	
ART UNIT	**PAPER NUMBER**
2642	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,274	OIDA ET AL.	
	Examiner	Art Unit	
	Thjuan P Knowlin	2642	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/19/01;01/24/02;02/10/03;12/17/03;04/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugaya et al (US 6,538,210).

2. In regards to claims 1, 5, 6, 11, 13, 17, 21, and 22, Sugaya discloses an RF module (circuit component built-in module and col. 5 lines 44-51) comprising; a multi-layered substrate (electric insulating substrate 101); a base-band IC, a memory IC, and an RF-IC mounted on said multi-layered substrate (col. 11 lines 53-60, col. 24-25 lines 66-7, and col. 29 lines 32-40); an RF passive component incorporated in said multi-layered substrate (col. 11 lines 53-60); and a wiring pattern (wiring patterns 102a and 102b) incorporated in said multi-layered substrate, said wiring pattern interconnecting said base-band IC and said memory IC (col. 11 lines 32-52 and col. 12 lines 8-22).

3. In regards to claims 2, 10, 16, and 18, Sugaya discloses an RF module, further comprising an antenna (antenna switch 1501a) incorporated in said multi-layered substrate (col. 29 lines 32-33).

4. In regards to claims 3, 4, 19, and 20, Sugaya discloses an RF module, wherein at least one of said base-band IC, said memory IC, and said RF-IC is a bare chip (col. 11 lines 53-60).

5. In regards to claims 7 and 23, Sugaya discloses an RF module, further comprising at least one trimming electrode pattern disposed on a surface of a said multi-layered substrate and arranged to enable adjustment of frequency characteristics of the RF module (col. 5 lines 12-18 and col. 8 lines 44-49).

6. In regards to claims 8 and 24, Sugaya discloses an RF module, wherein said RF-IC is a bare chip (col. 11 lines 53-60), and said RF module further comprising: a ground pattern arranged to prevent RF signal radiation provided within said multi-layered substrate at a location on the bottom surface of said bare chip, so as to prevent unnecessary radiation of RF signals from said RF-IC; and a plurality of via holes arranged within said multi-layered substrate and around said bare chip, said via holes providing connection to said ground electrode pattern for preventing RF signal radiation (col. 8 lines 21-33, col. 14 lines 26-39, and col. 15 lines 36-57).

7. In regards to claims 9 and 15, Sugaya discloses an RF module, further comprising a metallic case disposed on said multi-layered substrate (col. 15 lines 36-50).

8. In regards to claim 12, Sugaya discloses an RF module, wherein the substrate is a multi-layered substrate made of ceramic material (col. 8 lines 44-49 and col. 12 lines 43-47).

9. In regards to claim 14, Sugaya discloses an RF module, wherein the surface mounted components includes at least one of a chip-type inductor, a chip-type capacitor, a chip resistor, a chip-type transistor, and a chip-type diode (col. 11 lines 53-60).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Degani et al (US 6,734,539) teach a stacked module package. Akamine et al (US 6,463,267) teach a high frequency power amplifying apparatus having amplifying stages with gain control signals of lower amplitudes applied to earlier preceding stages. Akamine et al (US 6,658,243) teach a high frequency power amplifying apparatus having amplifying stages with gain control signals of lower amplitudes applied to earlier preceding stages.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thjuan P Knowlin whose telephone number is (703) 308-1727. The examiner can normally be reached on Mon-Fri 8:00-4:30pm.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ahmad Matar can be reached on (703)305-4731. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thjuan P. Knowlin

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